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During this AASERT program, we have carried out the fabrication and evaluation of high speed receiver circuits implemented with this technology. To demonstrate the provideing a bandwidth of 9GHz and an 8x8 III-V active-pixel sensor array with 285 MHz operation. In the following we present a complete characterization of this smart pixel technology, including the S- and Y-parameters extraction for the typical devices implemented by this technolgy.

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April 19, 1999

NE

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Dear Vicky Percy,

Enclosed is the Final Technical Report for Grant number F49620-941-0340, under Dr. Sadik Esener supervision. For any technical ~~questions please contact Dr.~~ Sadik Esener.

Sincerely,

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Final Technical Report

for

Technological Development for Interfacing Parallel Access Memories to Parallel Computers

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1. *Objectives and Accomplishments*

The main objective of this program that was funded in conjunction with the AFOSR F49620-94-1-0171 parent program was the development of a smart-pixel technology capable of interfacing parallel optical memories via massively parallel optical interconnects to computing systems at high speeds. To this end we have developed a monolithic smart pixels technology integrating MQW modulators, and detectors operating at 1.06μm wavelength with high speed MODFETs. OE Chips fabricated with this technology can be easily integrated via flip-chip bonding with silicon CMOS chips. During this AASERT program, we have carried out the fabrication and evaluation of high speed receiver circuits implemented with this technology. To demonstrate the applicability of this technology we have implemented a transimpedance receiver circuit providing a bandwidth of 9GHz and an 8x8 III-V active-pixel sensor array with 285 MHz operation. In the following we present a complete characterization of this smart pixel technology, including the S- and Y-parameters extraction for the typical devices implemented by this technology.

2. *Monolithic integration of III-V OE circuits and Their Performance*

2.1 Monolithic integration technique

The objective of the work was to develop small-scale integration of high-speed III-V optoelectronic devices and then flip-chip bond them to silicon-VLSI circuitry. The monolithic integration technique that we developed for Smart Pixels integration is based on InAlGaAs/InGaAs MQW materials on GaAs substrates.

For optical I/O we used InAlGaAs/InGaAs MQW light modulators operating around 1.06 μm wavelength. Since GaAs substrates are transparent at this wavelength, the integrated III-V circuits can be flip-chip bonded to silicon VLSI chips without removing the GaAs substrate. The lattice mismatch between the InAlGaAs/InGaAs MQWs and the GaAs substrate was accommodated by the insertion of compositionally step-graded InAlGaAs buffer layers with increasing indium composition. In this material system, we are also able to use InGaAs with high indium content in the FET channel to enhance the electronic device performance. Figure 1 shows the material layer structure. It is designed such that a modulation-doped FET channel is inserted into the n-contact layer of a MQW PIN device; the structure permits the fabrication of both devices from the same epitaxial layers. Both enhancement-mode and depletion-mode MODFETs have been fabricated using the same epitaxial layers. The use of enhancement-mode and depletion-mode devices allows the design of low-power logic circuits for optoelectronic applications.

2.2 DC characteristics

The devices were characterized using different size enhancement and depletion mode FET structures. The DC measurements included I-V, gate current and g_m measurements. Figure 2 and 3 show the measured DC characteristics for a double heterostructure silicon delta-doped InAlAs/InGaAs pseudomorphic HEMTs. Fairly large transconductance near 400 mS/mm were measured for the enhancement-mode devices

and over 300 mS/mm for the depletion-mode devices. The maximum current density was approximately 300 mA/mm for the device.

delta-doping

n+	$In_{0.25}Ga_{0.75}As$	cap layer	100A
n	$In_{0.25}Al_{0.75}As$	quasi-insulator	300A
i	$In_{0.25}Al_{0.75}As$	spacer	30A
i	$In_{0.15}Ga_{0.85}As$	channel	150A
i	$In_{0.25}Al_{0.35}Ga_{0.40}As$	spacer	350A
i	$In_{0.25}Al_{0.35}Ga_{0.40}As$/ $In_{0.25}Ga_{0.75}As$	MQWs	50x(60A/100A)
p+	$In_{0.25}Al_{0.35}Ga_{0.40}As$	buffer layer	5000A
i	$In_{0.15}Al_{0.35}Ga_{0.50}As$	buffer layer	5000A
i	GaAs	substrate	

Figure 1: Material structure for an integrated MODFET and MQW pin modulator/detector

One of the concerns in III-V MESFET and MODFET technology is the gate leakage which occur under reverse and forward bias conditions. With the use of the large bandgap quasi-insulator $In_{0.25}Al_{0.75}As$ these effects are significantly reduced. For some of the enhancement-mode $In_{0.25}Al_{0.75}As/In_{0.25}Ga_{0.75}As$ MODFETs, gate-source voltages of up to 1.25 V could be applied without significant gate leakage. In addition, excellent reverse gate drain diode characteristics were measured and are plotted in Figure 4. The gate drain breakdown was over 20 V if one specifies the breakdown current density to be 10 μA/μm.

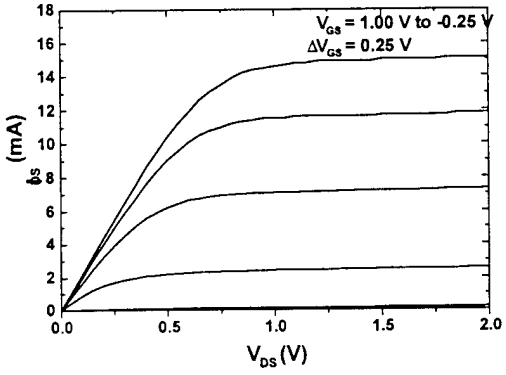


Figure 2: Drain I-V characteristics for a 1.0x50 μm^2 enhancement-mode $In_{0.25}Al_{0.75}As/In_{0.25}Ga_{0.75}As$ MODFET

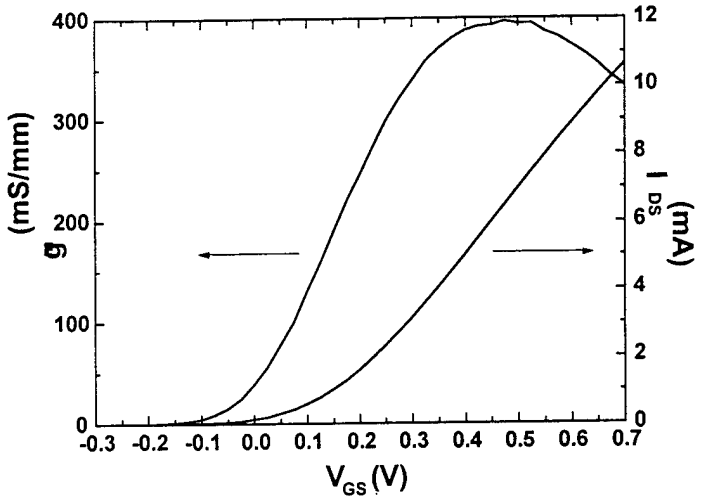


Figure 3: g_m and I_{DS} as functions of V_{GS} for a 1.0 x 50 um^2 $In_{0.25}Al_{0.75}As/In_{0.25}Ga_{0.75}As$ MODFET

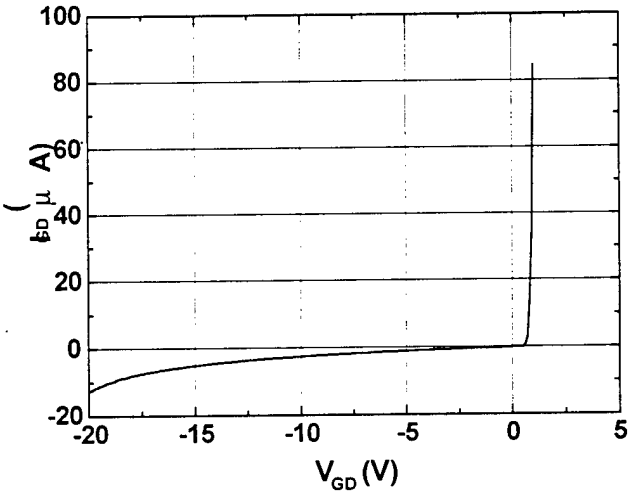


Figure 4: I_{GD} as functions of V_{GD} for a 1.0 x 50 um^2 $In_{0.25}Al_{0.75}As/In_{0.25}Ga_{0.75}As$ MODFET

2.3 RF parameter extraction

2.3.1 MODFETs

Many different small-signal circuit topologies can be used for modeling the properties of FETs. Though the extrinsic parasitic elements may slightly differ in their placement in the equivalent circuit, the intrinsic transistor model is usually the same. The general description of the small circuit equivalent circuit is shown in Figure 5. A unique

feature of the material layer structure used in this technology is that there is an underlying p-layer to raise the electron potential from the substrate side so that the electrons are confined in the channel region. To account for this feature, the drain-source capacitor (C_{DS}) is modified as shown in Figure 6.

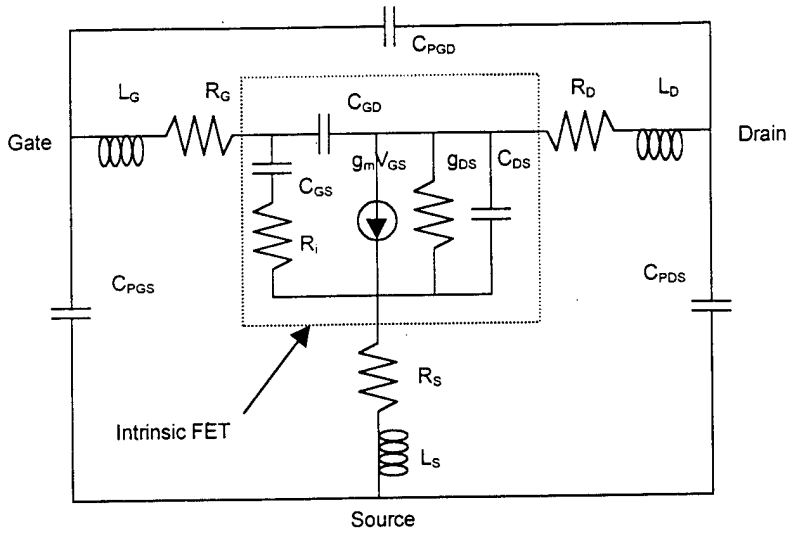


Figure 5: Equivalent circuit representation of a FET

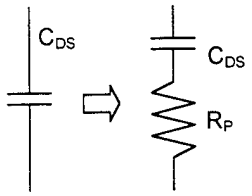


Figure 6: Modified small signal representation to account for underlying p-layer

The extrinsic elements were first determined by using transmission line model for the resistances and inductances and the FETs pinched-off for capacitances. The results are summarized in Table 1. The S-parameters were measured at various bias points across the different regions of operation for the FETs from 0.5 to 26GHz. S-parameter measurements and curve fitting then determined the intrinsic parameters. Table 2 summarizes the intrinsic parameters and Figure 7 includes the S_{11} and S_{22} smith chart.

Table 1: Summary of extrinsic parameters

L_G (nH)	L_D (nH)	L_S (nH)	R_G (Ω)	R_D (Ω)	R_S (Ω)	C_{GDP} (fF)	C_{DSP} (fF)	C_{GSP} (fF)
35.6	15.0	1.5	1.1	16.38	9.18	4.29	21.40	22.10

Table 2: Summary of intrinsic parameters (V_{GS} = 0.5 V, V_{DS} = 1.5 V) for a 1.0x50 um^2 $In_{0.25}Al_{0.75}As/In_{0.25}Ga_{0.75}As$ MODFET

C_{GS} (fF)	C_{GD} (fF)	C_{DS} (fF)	Rp (Ω)	R_i (Ω)	g_m (S)	g_{ds} (S)	τ (psec)
138.19	1.01	38.20	60.70	9.42	2.40E-02	5.41E-04	2.15

The unity current gain frequency (f_T), a common figure of merit, is 27GHz based on our measurement results. In summary, the device demonstrates good performance despite the buried p-layer underneath the FET. Parasitic capacitance is fairly small because of the separation of p-layer to the modulation-doped channel.

2.3.2 PIN diodes

The pin structures were modeled with inductance and capacitance associated with the microwave pads and the common representation of a PIN diode shown in Figure 8. Table 3 lists the extracted parameters for two types of modulator structures. The M50A is an approximately 50x50 μm^2 pin structure whereas the M22B is a much smaller 22x22 μm^2 structure. In general, for the pin structures, the depletion capacitance scaled

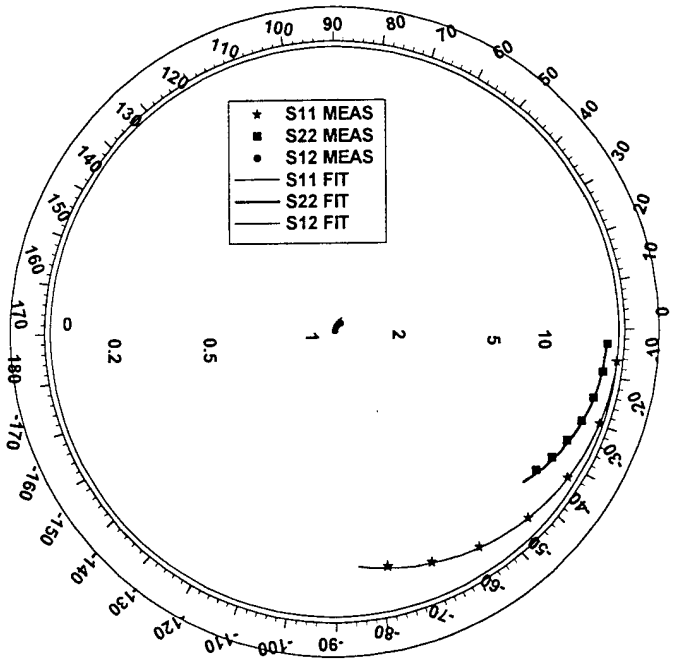


Figure 7: S_{11} and S_{22} smith chart of MODFET (measurements and data fitting)

directly with area. Also, the series resistance for the pin structures increased as the device size shrank due to the decreasing ohmic contact areas. However, in this particular case the M22B was a device that was entirely surrounded by the p-contact, whereas the M50A only had three sides of the mesa that had ohmic contact to the p-layer.

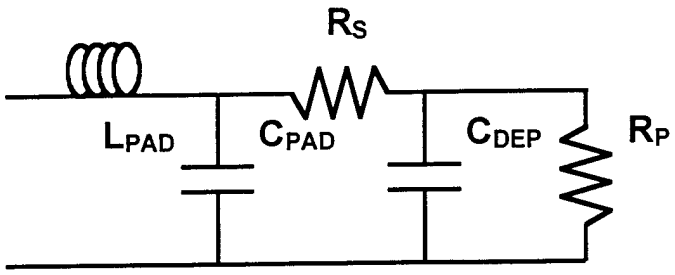


Figure 8: Equivalent circuit representation of a PIN diode

Table 3: Model parameters for two types of photodiode structures

	L_{PD} (nH)	C_{PD} (fF)	R_S (Ω)	C_{DEP} (fF)	R_P (Ω)
M50A	21.8	22.4	41.8	438.4	11386
M22B	21.1	21.0	35.4	88.0	26152

The 3-dB bandwidth, f_{3dB}, is calculated from R_S and C_{DEP} taking into account the influence of the large microwave pad parasitics. The reduction of the depletion capacitance by scaling the devices to smaller dimensions increased the bandwidth significantly. Also, from the graph, one can observe the large impact of series resistance on the bandwidth. Two sets of data from two different samples are shown in the figure below (Figure 9) where R_S varied by a factor of two. This effect was primarily due to the series resistance of the p layer and the p ohmic contact that dominated R_S.

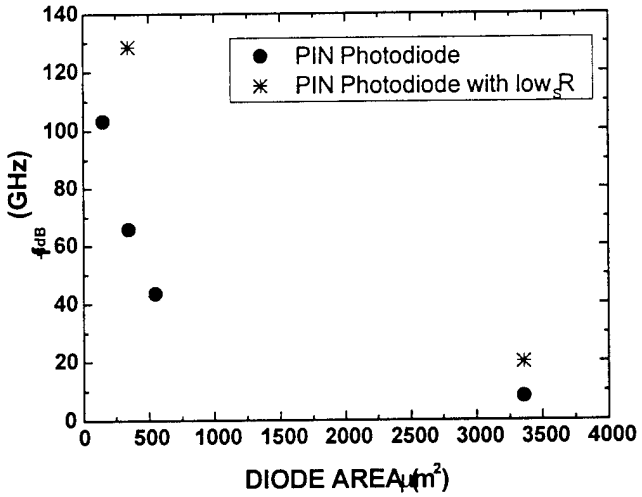


Figure 9: 3-dB bandwidth versus photodiode area from various fabricated diode structures

2.4 Transimpedance receiver

The receiver circuit was based on a transimpedance amplifier design shown in Figure 10. The first stage is a transimpedance stage with a common source stage buffered by a source follower stage and an adjustable FET providing resistive feedback to the input. This first stage provides conversion of the photocurrent generated in the photodiode into a voltage that is amplified by the preceding common-source stage. The output is further amplified further by two more source follower stages which level shift and reduce the output resitance so that a 50-ohm output can be easily driven. Note the distinction between enhancement mode devices (black) and depletion mode devices (shaded) facilitated by our fabrication approach..

Varying the feedback resistance (via V_{FB}) affects the transimpedance gain of the circuit as well as the bandwidth. The graph in Figure 10 illustrates the effects of various feedback resistances on the output characteristics of the transimpedance stage with the larger resistance reducing the required optical power. Figure 11 shows the closed loop transfer characteristics of the circuit measured under DC conditions. The resistance is estimated from scaling a larger depletion device. Differences between the response of the simulated and measured circuits lies in the fact that the fabrication results varied from sample to sample and in between processing steps. Our device characteristics exhibited a very large standard deviation due to the limitations imposed by our wafer quality and uniformity achieved during various micro-fabrication processes. The average depletion devices exhibited a $g_m \sim 210$mS/mm. An over etch of the depletion mode devices resulted in a threshold that was near –0.5 V. much more enhancement than previous devices. In addition, the circuits were biased at V_{DD} =2.0 V limited by avalanche breakdown.

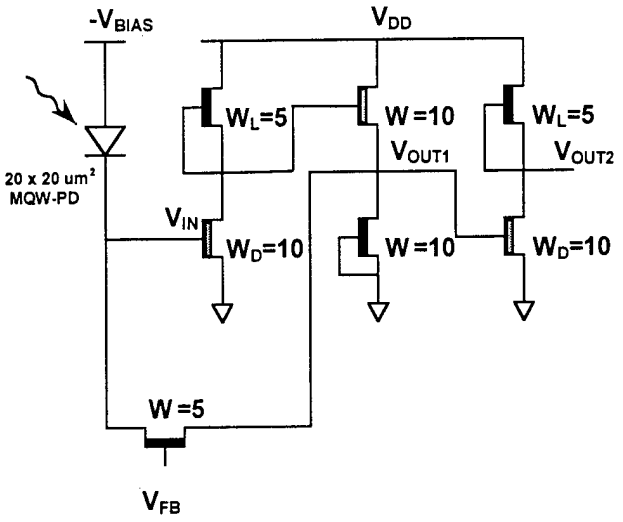
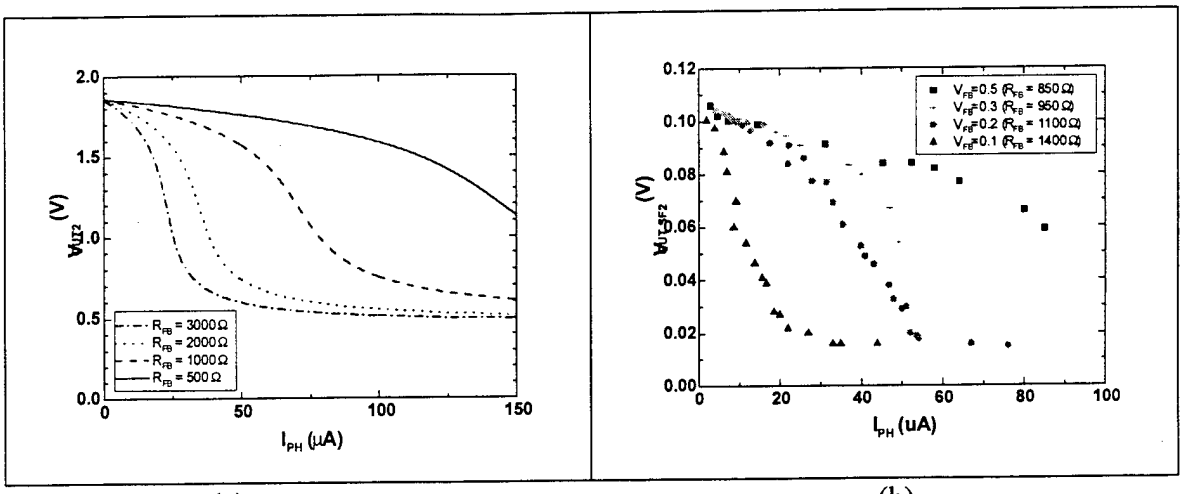


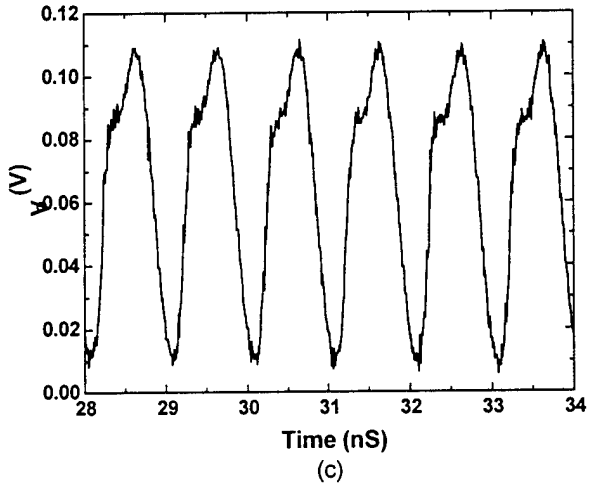
Figure 10: Transimpedance receiver circuit



(a) (b)

Figure 11 a) Simulated closed loop characteristics of the receiver circuit for various feedback resistance. b) Measured closed loop characteristics of the receiver circuit

The high-frequency performance of the receiver was measured using a digital laser source at 850nm with a bandwidth of 1 GHz. This laser module was driven by a HP high-frequency digital source with a bandwidth of 3 GHz. The measured receiver output was fairly constant till 1GHz where the measured output signal started to drop significantly. This happened for all the feedback voltages indicating the limiting bandwidth was that of the driver laser diode. However, the output would follow the input modulation up to 2.5 GHz despite the shrinking waveform. Figure 12 is the transient response of the receiver at 1GHz.



(c)

Figure 12: Receiver circuit transient response at 1 GHz

To estimate the bandwidth of the transimpedance receiver, we used the extracted device parameters and the the transfer function

$$H(\omega) \cup \frac{-R_F}{1 + j\omega R_F \frac{C_D + C_{IN}}{A} + C_F}.$$

The corresponding equivalent circuit shown in Figure 13 was used to extract device parameters. The large dc gain, $A \sim g_m/g_o$, of the common-source circuit is approximately 30 to 40 primarily because of the low output conductance of these MODFETs. The input capacitance, C_{IN}, of the common source amplifier in the transimpedance stage is estimated to be about 60fF from the gate source capacitance and the miller effect capacitance. The photodiode depletion capacitance, C_D, for a $20x20\mu m^2$ device is approximately 80fF. The feedback capacitance is dependent on the drain-source capacitance of the tunable 5μm MODFET which is approximately 4.3fF. Thus, for a transimpedance (feedback resistance) in the low kilo-ohm range the bandwidth would be in the 5 to 9 GHz range.

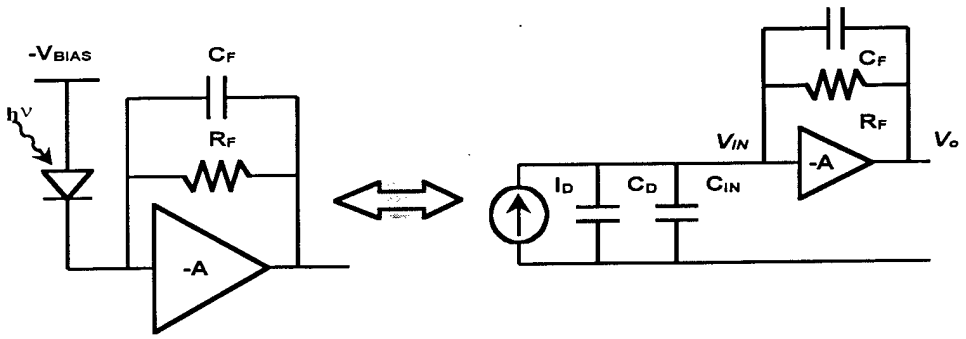


Figure 13 Equivalent circuit representation of a transimpedance amplifier

3. Summary

In this program, a complete characterization of a monolithic optoelectronic array technology has been carried out. RF performance of the typical devices fabricated using this technology has been evaluated based on the s-parameter extraction from the devices. The measured bandwidth of the devices was around 9GHz. These devices led to the operation of a a transimpedance receiver circuit which exhibited a bandwidth of at least 1GHz limited by our measurement tools.

4. Related publications

D. Shih, H. Sari, C. Fan, and S. C. Esener, "Monolithically Integrated MQW Modulator and MODFET OE Circuits for flip-chip bonding with CMOS," *Technical Digest on OSA Topical Meeting on Spatial Light Modulators,* Lake Tahoe, NV, March 1997.

D. A. Van Blerkom, C. Fan, M. Blume, and S. C. Esener, "Transimpedance receiver design optimization for smart pixel arrays," *IEEE Journal of Light Wave Technology*, Vol. 16, pp119126, 1998.

Chi Fan, David W. Shih, Mark W. Hansen, Daniel Hartman, Daniel Van Blerkom, Sadik C. Esener, and Michael Heller, "Heterogeneous integration of optoelectronic components," *SPIE Proceeding,* Vol. 3290, 1998.